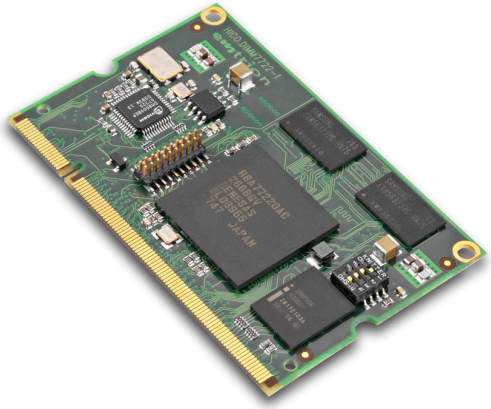
HiCO.DIMM7722

Processor Module with SH7722

Hardware Description



emtrion

This document is published by:

emtrion GmbH
Greschbachstr. 12
D-76229 Karlsruhe
http://www.emtrion.com

Tel: +49 721 62725-20
Fax: +49 721 62725-19
E-mail: mailto:mail@emtrion.de

October 2008 - 002

Revision History

Revision No.	Changes	Date
1	First revision	2008-07-29/ Bue
2	CPU clock changed to 330 MHz, maximum current consumption increased to 350 mA, several chapters added and some literal errors corrected	2008-10-06 / Bue

Table of Contents

1. Introduction

The HiCO.DIMM7722 processor module is a SODIMM sized CPU board based on the SuperH SH4AL-DSP processor SH7722 from Renesas.

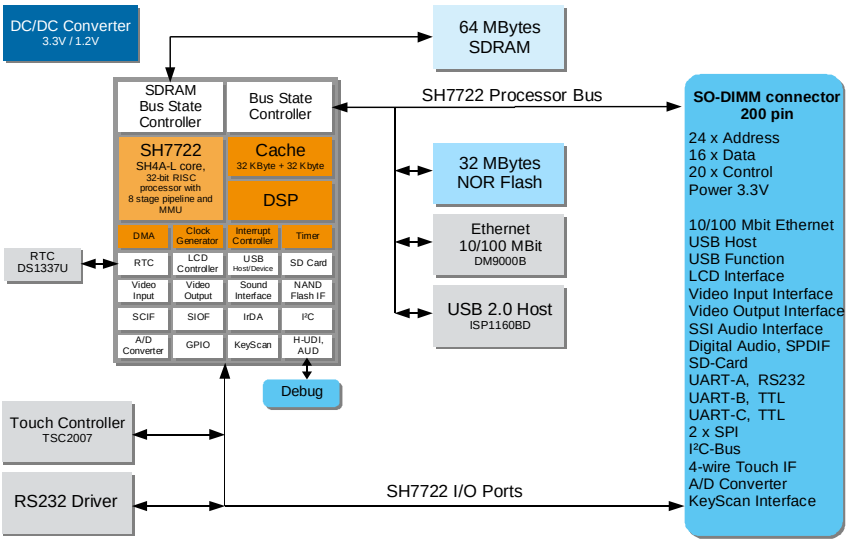
The processor core runs at 330 MHz and it includes a variety of functions required for multimedia applications. These include MPEG4 and H.264 accelerators, a 2D graphics accelerator, LCD controller, camera interface, and sound input/output module.

The module comes with 32 MB NOR-Flash and 64 MB of SDRAM. In addition to the processor and the memory, a 10/100-Mbps Ethernet controller, a USB Host controller and a touch controller are available.

All interfaces are accessible through the 200 pin SODIMM edge connector which complies mechanically with SODIMM memory sockets with 2.5 V keying.

The power consumption of the whole board is less than 1 W.

2. Block Diagram



3. Handling Precautions

Please read the following notes prior to installing the HiCO.DIMM7722 processor module. They apply to all ESD (electrostatic discharge) sensitive components:

- The HiCO.DIMM7722 does not need any configurations before installation.
- The module does not provide any on-board ESD protection circuitry – this must be provided by the product it is used in.
- Before installing the module it is recommended that you discharge yourself by touching a grounded object.
- Be sure all tools required for installation are electrostatic discharged as well.
- Before installing (or removing) the module, unplug the power cable from your mains supply.
- Handle the board with care and try to avoid touching its components or tracks.

4. Functional Description

4.1. Processor

The HiCO.DIMM7722 processor board uses the SuperH SH4AL-DSP processor SH7722 from Renesas [1], a 32–bit RISC processor which runs at 330 MHz.

In addition to the CPU core with MMU and Caches, this processor provides a lot of features especially needed for Multimedia applications such as:

- DSP with six 32-bit data registers, two 40-bit data registers and 16 KB X/Y memory
- Interrupt controller with 15 levels and nine external interrupt pins
- Bus state controller with SRAM, Burst ROM, SDRAM and PCMCIA interface
- 6-channel DMA controller with two external inputs
- Three 32-bit auto-reload timers
- Two SIOs with 64 byte FIFO
- Three UARTs with 16 byte FIFO and high speed mode
- I2C bus interface
- Video input module with camera capturing module and image processing unit
- Video output unit, digital outputs conform to ITU-R BT.601, ITU-R BT.656
- Video processing unit for MPEG-4 H.264 encoding and decoding
- JPEG processing unit
- LCD Controller for TFT displays up to SVGA and 24 bpp
- 2D graphics accelerator
- Sound interface with PCM and I2S format
- USB 2.0 Device with high-speed mode
- SD Card host controller
- Key scan interface for up to 30 keys
- H-UDI debug interface

Further details of the processor can be found in the SH7722 hardware manual [1].

4.2. Flash

The HiCO.DIMM7722 contains 32 MByte NOR flash which serves as program and data storage memory. A flash memory PC28F256P33 from Intel is used and connected to the 16-bit wide data bus.

The flash device is located in area 0 from 0x00000000 ... 0x01FFFFFF.

4.3. RAM

64 MByte SDRAM are available as main memory. The memory consists of two 256 MBit SDRAMs, type 2M*32*4, that are connected in parallel to a 64-bit wide data bus. They are clocked at 133 MHz and operated with CAS3.

The RAM is located in area 3, in the address range 0x0C000000 … 0x0FFFFFFF.

4.4. Ethernet Controller

The Ethernet interface is driven by the DM9000B Ethernet controller from Davicom [2]. This controller comes with the Media Access Controller (MAC) and Physical Layer Interface (PHY) on a single chip.

A 16 Kbytes on-chip SRAM serves to buffer transmit- and receive frames. The chip is able to put itself to the operating modes 100BASE-TX or 10BASE-T, both half- and full duplex. Also HP Auto-MDIX is supported.

The MAC and configuration data of the Ethernet controller are stored in a 93C46 type EEPROM.

The Ethernet controller uses two addresses in area 5B of the processor. The index port is located at 0x16000000 and the data port at 0x16000002. The interrupt output of the Ethernet controller is connected to IRQ5.

The Ethernet signal lines as well as two status signals that serve to indicate the link status and the transfer speed are connected to the SODIMM connector. An appropriate 1:1 transformer must be added externally.

4.5. USB Host

A USB Host interface is used to connect USB devices such as a keyboard, mouse, printer or memory stick.

The USB host interface is realized by the host controller ISP1160 from Philips [3]. It complies with the USB specification Rev. 2.0, supporting data transfers at low-speed- and full-speed. From the two downstream ports only the first one is used. The port has an overcurrent detection input and a power supply switching control output.

In PIO mode the ISP1160 occupies two addresses in area 5A. The 16 bit data port at address 0x15000000 and the command port at address 0x15000002. The interrupt output is connected to IRQ3. DMA transfers can be done using DMA channel 0.

The data lines and the two control lines are available at the SODIMM connector. A USB power switch must be added externally. The data lines are internally terminated with 15-KΩ pulldown resistors.

4.6. USB Function

The USB function port allows the data exchange with an external host.

The interface is realized by the internal controller of the SH7722. It complies with the USB specification Rev. 2.0, supporting data transfers at low-speed-, full-speed ad high-speed.

The data lines and the VBUS input are available at the SODIMM connector.

4.7. LCD and Video Output

The SH7722 includes an integrated LCD controller and a video output unit (VOU) which share the same processor pins.

4.7.1. Video Output Unit

The video output unit (VOU) supports the video system NTSC with a maximum image size of 720 x 240 dots. The provided output interfaces are 16-bit Y/C interface or 8-bit multiplexed YC interface.

All data and control lines are available at the SODIMM connector. A 27 MHz source clock for the video output unit must be supplied from the base board.

4.7.2. LCD Display

The LCD controller of the SH7722 can drive TFT displays with resolutions up to SVGA at 18 bpp. The pixel clock for the display data is normally generated internally by a special pattern generator but can also be sourced externally.

All data and control lines for displays with 18 bit colour depth are available at the SODIMM connector.

4.7.3. Display Destination and Reset

Since both output interfaces share their pins they can't be used simultaneously.

Therefore the port pin PTT0 is available as signal VOU_DEST on the SODIMM connector. This signal is reserved to select the output destination on carrier boards with both options.

Additionally the port pin PTW4 is available on the SODIMM as signal VOU_RST#. This signal is reserved to reset an external video codecs on a carrier board.

4.8. Touch Interface

A 4-wire touch interface is implemented using the touch interface controller TSC2007 from Texas Instruments [4]. The touch controller is connected to the I²C bus interface of the SH7722. The pen interrupt is connected to IRQ1.

Besides the touch interface the TSC2007 can also measure the analog voltage input ANA_IN1 at the SODIMM interface. This input has an input voltage range of 0 V … 3.3 V with 12 bit resolution.

The touch interface signals are available at the SODIMM connector.

4.9. Video Input

The SH7722 includes a video input unit (VIO) which can be used to capture data from different video sources, such as a video codec or a CCD camera module.

The interface of the HiCO.DIMM7722 is realised with an 8-bit data-bus available at the SODIMM connector and supports various input formats. The clock must be supplied externally via the SODIMM connector.

To switch between two different video sources the port pin PTT2 is available as signal VIO_SRC at the SODIMM connector. To reset a video codec on the base board the signal VIO_RST can be used. It is driven by the port pin PTT3.

4.10. Audio Interface, SSI port

The SH7722 processor has an integrated sound interface, SIU (Sound Interface Unit). The interface can be used to connect external audio Codecs via an SSI connection or it can drive directly digital audio data conforming to the SPDIF format.

The interface is connected to SODIMM connector, which allows the connection of an external audio codec. The input clock for the sound interface must be externally supplied.

4.11. SD-Card Interface

The SH7722 includes an SD Card interface to connect memory cards or SDIO cards. All signals are available at the SODIMM connector.

4.12. Serial Ports

The HiCO.DIMM7722 comes with three serial ports which are all integrated in the processor. They all have 16 byte FIFOs and are equipped with modem control lines RTS and CTS.

SCIF0 and SCIF2 are directly available at the SODIMM connector with LVTTL level, SCIF1 is also available at the SODIMM connector but with RS232 compatible signals.

4.13. RTC DS1337

Since the integrated RTC of the processor SH7722 does not have a separate power supply the RTC DS1337 from Maxim is added. It is clocked by a 32.768 KHz crystal which also serves as clock source for the processor.

The DS1337 is connected to the I²C bus interface of the SH7722. An alarm interrupt is not available.

Via the SODIMM connector the RTC can be buffered by an external battery. For timekeeping a supply voltage between 1.3 Volt and 3.3 Volt must be supplied. The current consumption is below 0.6 µA.

4.14. DIP Switches, Status LED

Four DIP Switches can be read via the port pins PTA[4:1] of the SH7722. If a switch is ON the corresponding bit is read as 1. If it is OFF the bit is read as 0.

A bicolour LED is connected to the port pins PTJ7 and PTJ5 of the SH7722. If PTJ7 is high a red LED is lighting, if PTJ5 is high a green LED is lighting. If both ports are high both LEDs are on, which results in a yellow light.

4.15. Memory Map

The SH7722 processor provides 8 areas with 64 MB address space whose characteristics can be individually programmed. The address usage is as follows:

Area	Function	Bus Width	Address Region
0	32 Mbyte Flash	16-bit	00000000 – 01FFFFFF
1	SH7722 intern	-	04000000 – 07FFFFFF
2	SH7722 intern	-	08000000 – 0BFFFFFF
3	64 MB SDRAM	64-bit	0C000000 – 0FFFFFFF
4	SODIMM	8/16-bit	10000000 – 13FFFFFF
5A	USB Host ISP1160	16-bit	14000000 – 15FFFFFF
5B	Ethernet DM9000B	16-bit	16000000 – 17FFFFFF

6A	SODIMM, CE2B#	8/16-bit	18000000 – 19FFFFF
6B	SODIMM, CE1B#	8/16-bit	1A000000 – 1BFFFFF
7	reserved	-	1C000000 – 1FFFFFF

The timing characteristics of all areas but areas 4, 6A and 6B are programmed according to the requirements of the HiCO.DIMM7722 processor board.

Areas 4, 6A and 6B are reserved for external extensions and therefore configured with the slowest timing.

4.16. Interrupts

The processor SH7722 has an integrated interrupt controller that analyzes all interrupt sources, prioritizes them and outputs the interrupt with the highest priority to the processor.

Six dedicated interrupt input pins are available for external devices. Besides these some GPIO pins can also be used to generate interrupts.

Three interrupts lines are used for the USB Host, the touch controller and the Ethernet controller, therefore two normal interrupts and the NMI are available for external devices via the SODIMM connector.

The use of the interrupt inputs and the resulting interrupt code is displayed in the following table:

Name	Source	INTEVT
NMI	SODIMM	0x1C0
IRQ0	SODIMM	0x600
IRQ1	Touch controller TSC2007	0x620
IRQ2	not available	0x640
IRQ3	USB Host ISP1160	0x660
IRQ4	not available	0x680
IRQ5	Ethernet controller DM9000B	0x6A0
IRQ6	KEYIN0 (SODIMM)	0x6C0
IRQ7	SODIMM	0x6E0

4.17. DMA

The SH7722 has an integrated DMA controller with six channels

Many integrated peripherals of the processor SH7722 like the Sound Unit, SD Card Controller, USB Device can be operated internally with DMA transfers.

Only channel 0 can receive external requests. This is used onboard for the USB Host ISP1160.

There is no DMA channel available at the SODIMM connector.

4.18. I²C- Bus

The SH7722 provides an I²C bus interface with transmission speeds up to 400 kb/s. The interface operates as a master.

Two devices are already connected on the HiCO.SH7722:

Slave	Device	Chip Address
Real Time Clock	DS1337U+	0x68
Touch Controller	TSC2007	0x48

The signal lines are available at the SODIMM connector.

4.19. Digital I/Os, Analog In

The SH7722 includes a Key Scan Controller block which can be used to connect a keyboard. Six output lines and four input lines are available at the SODIMM connector. The pins can be either used as a keyboard interface for up to 24 keys or used as GPIOs. Details how the port pins can be used are documented in the SH7722 hardware manual [1].

One analog input ANA_IN1 is available at the SODIMM interface. The input has a voltage range of 0 V … 3.3 V with 12 bit resolution. The analog input is part of the touch controller.

4.20. SPI

The SH7722 includes two synchronous serial interfaces SIOF which are configured as SPI interface. The signals from both interfaces are available at the SODIMM connector.

4.21. Reset

There are several ways for issuing a reset signal:

- Two voltage monitors check the 3.3 Volt supply voltage of the board and the 1.2 Volt Core voltage of the processor.
- Via the active low signal RESBASE# at the SODIMM connector
- Via the active low signal HRESI# at the Debug connector
- Via software by setting port pin PTJ6 to 1

All resets are hardware resets of the whole board and issue a Power-on reset of the processor.

The duration of the reset signal is min. 100 ms. For resetting external devices the reset signal is available as an output at the SODIMM connector.

4.22. Debugging interface

At the 20 pole header J1 all signals of the User Debugging Interface H-UDI and also the additional six pins for emulator connection, AUD, are available.

Please contact emtrion for further details how to connect an emulator to J1.

4.23. Power Supply

A voltage of +3.3 volts, +/- 5%, @ max. 0.5 A should be supplied via the SODIMM connector. Further voltages for the processor and the other parts are generated on board.

4.24. HiCO.DIMM Interface

All interface signals of the board and an SRAM like bus interface for external peripheral additions are available at the SODIMM connector which is named HiCO.DIMM interface.

The HiCO.DIMM interface is a 200 pos SODIMM connector that fits mechanically into a regular DDR1 SODIMM memory socket with 2.5V keying. These sockets are available from various manufacturers.

Usage details of the connector and its electrical and mechanical characteristics can be found later in this document.

Watch:

The pinout of the SODIMM connector is NOT compatible with memory sockets. Insertion into a socket with wrong pinout may damage the HiCO.DIMM7722 and the carrier board.

Notes:

- The pins 29, 31, 119, 121 can serve as SCIF0 modem control lines or SPDIF signal lines. Only one of these functions is available, depending on the software.
- The Video Output interface and the LCD interface share the pins 41 ... 76 of the SODIMM connector. Some of the pins change their behaviour and name according to the active interface.
- Most of the pins are directly connected with the processor SH7722. For detailed electrical specification please refer to Section 43, Electrical Characteristics, in the SH7722 hardware manual [1]

5. Pin Assignments

5.1. J1, Debugging Connector

Type 20-pin connector, Samtec FTSH-110-01-FM-DV-K-P

Pin	Signal	Pin	Signal
1	AUDCK	**2**	TCK
3	GND	**4**	GND
5	AUDSYNC	**6**	TRST#
7	+3.3 V	**8**	+3.3 V
9	AUDATA3	**10**	TDO
11	AUDATA2	**10**	ASEBRK#
13	AUDATA1	**10**	TMS
15	AUDATA0	**10**	TDI
17	GND	**18**	MPMD
19	HRESI#	**20**	RESET#

5.2. J2, HiCO.DIMM

Type SODIMM, 200 pos, 2.5V keying

Pin	Signal	Interface		Signal	Pin
1	SPEED_LED#	Ethernet	USB Host	USBH_PEN#	2
3	ETH_TDP			USBH_OC#	4
5	ETH_TDM			USBH_DM	6
7	GND			USBH_DP	8
9	ETH_RDP		USB Device	USBF_VBUS	10
11	ETH_RDM			USBF_DM	12
13	LINK_LED#			USBF_DP	14
15	+3V3	Power		GND	16
17	n/c		UART	SCIF1_TXD#	18
19	n/c			SCIF1_RXD#	20
21	SCIF2_TXD	UART		SCIF1_RTS#	22
23	SCIF2_RXD			SCIF1_CTS#	24
25	SCIF2_RTS		Touch	Touch_XP	26
27	SCIF2_CTS			Touch_XM	28
29	SCIF0_RTS (SPDO)**	UART		Touch_YP	30
31	SCIF0_CTS (SPDI)**			Touch_YM	32
33	SCIF0_TXD		A/D	ANA_IN1	34
35	SCIF0_RXD			n/c	36
37	n/c	A/D		n/c	38
39	+3V3	Power		GND	40
41	LCD_D22	LCD, VOU		LCD_D23	42
43	LCD_D20			LCD_D21	44
45	LCD_D18 / DV_CLKO			LCD_D19 / DV_CLKI	46

47	LCD_D16 / DV_VSYNC		LCD_D17 / DV_HSYNC	**48**
49	LCD_D14 / DV_D14		LCD_D15 / DV_D15	**50**
51	LCD_D12 / DV_D12		LCD_D13 / DV_D13	**52**
53	LCD_D10 / DV_D10		LCD_D11 / DV_D11	**54**
55	LCD_D8 / DV_D8		LCD_D9 / DV_D9	**56**
57	LCD_D6 / DV_D6		LCD_D7 / DV_D7	**58**
59	LCD_D4 / DV_D4		LCD_D5 / DV_D5	**60**
61	LCD_D2 / DV_D2		LCD_D3 / DV_D3	**62**
63	LCD_D0 / DV_D0		LCD_D1 / DV_D1	**64**
65	+3V3		GND	**66**
67	n/c		LCD_LCLK	**68**
69	LCD_DISP		LCD_DCK	**70**
71	LCD_HSYN		LCD_DON	**72**
73	LCD_VSYN		LCD_VCPWC	**74**
75	VOU_DEST		LCD_VEPWC	**76**
77	VOU_RST#	**VIO**	VIO_D7	**78**
79	n/c		VIO_D6	**80**
81	n/c		VIO_D5	**82**
83	VIO_CLK2		VIO_D4	**84**
85	VIO_HD2		VIO_D3	**86**
87	VIO_VD2		VIO_D2	**88**
89	VIO_SRC		VIO_D1	**90**
91	VIO_RST#		VIO_D0	**92**

93	+3V3	**Power**		GND	**94**
95	SPI2_MISO	**SPI2**	**SDC**	SDC_D0	**96**
97	n/c			SDC_D1	**98**
99	n/c			SDC_D2	**100**
101	SPI2_SS#			SDC_D3	**102**
103	SPI2_MOSI			SDC_CMD	**104**
105	SPI2_SCK			SDC_CLK	**106**
107	n/c			SDC_CD#	**108**
109	n/c			SDC_WP#	**110**
111	SPI1_SS#	**SPI1**		SPI1_MISO	**112**
113	SPI1_SCK			SPI1_MOSI	**114**
115	SCL	**I2C**	**Audio**	AUDIO_BCK	**116**
117	SDA			AUDIO_LRC	**118**
119	SCIF0 CTS (SPDI)**	**(SPDIF)**		AUDIO_DATI	**120**
121	SCIF0 RTS (SPDO)**			AUDIO_DATO	**122**
123	GND	**Power**		AUDIO_MCLK	**124**
125	KEY_8	**GPIO**		KEY_9	**126**
127	KEY_6			KEY_7	**128**
129	KEY_4			KEY_5	**130**
131	KEY_2			KEY_3	**132**
133	KEY_0			KEY_1	**134**
135	+3V3	**Power**		GND	**136**
137	A22	**Address A[23:0]**		A23	**138**
139	A20			A21	**140**
141	A18			A19	**142**
143	A16			A17	**144**
145	A14			A15	**146**

147	A12		A13	**148**
149	A10		A11	**150**
151	A8		A9	**152**
153	A6		A7	**154**
155	A4		A5	**156**
157	A2		A3	**158**
159	A0		A1	**160**
161	+3V3	**Power**	GND	**162**
163	D14	**Data D[15:0]**	D15	**164**
165	D12		D13	**166**
167	D10		D11	**168**
169	D8		D9	**170**
171	D6		D7	**172**
173	D4		D5	**174**
175	D2		D3	**176**
177	D0		D1	**178**
179	CKIO	**Bus Control**	n/c	**180**
181	BS#		n/c	**182**
183	RD#		IRQ0	**184**
185	RD/WR#		IRQ7	**186**
187	WE0#		NMI	**188**
189	WE1#		RESO#	**190**
191	ICIORD#		RESI#	**192**
193	ICIOWR#		CE1B#	**194**
195	WAIT#		CE2B#	**196**
197	CS4#		IOIS16#	**198**
199	BAT	**Power**	GND	**200**

** Digital Audio interface is actually not available

6. Signal Characteristics

Abbreviations:

AI	analog input
AO	analog output
A I/O	analog bidirectional
I	digital input
O	digital output
I/O	digital bidirectional
IPU xK	digital input with x KΩ pullup resistor

Name	Direction	Volt [V]	Current [mA]	Description
Ethernet				
SPEED_LED#	O	3.3	4	100 MBit indicator
ETH_TDP	A O	-	-	TX diff. output pos.
ETH_TDM	A O	-	-	TX diff. output neg.
ETH_RDP	A I	-	-	RX diff. input pos.
ETH_RDN	A I	-	-	RX diff. input neg.
LINK_LED#	O	3.3	4	traffic indicator
USB Host				
USBH_PEN#	O	3.3	4	Power enable for switch
USBH_OC#	I	3.3	-	Overcurrent from switch
USBH_DP	I/O	3.3	-	Diff. data positive
USBH_DM	I/O	3.3	-	Diff. data negative
USB Device				
USBF_VBUS	I	5	-	VBUS detection
USBF_DP	I/O	3.3	-	Diff. data positive
USBF_DM	I/O	3.3	-	Diff. data negative
UART				
SCIF0_TXD	O	3.3	2	transmit data
SCIF0_RXD	I	3.3	-	receive data

SCIF0_RTS	O	3.3	2	modem control
SCIF0_CTS	I	3.3	-	modem control
SCIF1_TXD#	O	RS232	2	RS232 transmit data
SCIF1_RXD#	I	RS232	-	RS232 receive data
SCIF1_RTS#	O	RS232	2	RS232 modem control
SCIF1_CTS#	I	RS232	-	RS232 modem control
SCIF2_TXD	O	3.3	2	transmit data
SCIF2_RXD	I	3.3	-	receive data
SCIF2_RTS	O	3.3	2	modem control
SCIF2_CTS	I	3.3	-	modem control
4-Wire Resistive Touch Interface				
TOUCH_XP	A I/O	3.3	-	X plus terminal
TOUCH_XM	A I/O	3.3	-	X minus terminal
TOUCH_YP	A I/O	3.3	-	Y plus terminal
TOUCH_YM	A I/O	3.3	-	Y minus terminal
Analog Input				
ANAI1	A I	3.3	-	12 bit analog input
LCD/VOU (Video Output Unit)				
LCD_VCPWC	O	3.3	2	VCC power control
LCD_VEPWC	O	3.3	2	VEE power control
LCD_DON	O	3.3	2	LCD display enable signal
LCD_VSYNC	O	3.3	2	LCD frame sync output
LCD_HSYNC	O	3.3	2	LCD line sync output
LCD_LCLK	I	3.3	-	LCD controller input clock
LCD_DCK	O	3.3	2	LCD pixel output clock
LCD_D[23:20]	O	3.3	2	upper LCD colour data
LCD_D19 / DVI_CLKI	O/I	3.3	2	LCD colour bit 19 / VOU clock input
LCD_D18 / DVI_CLKO	O/O	3.3	2	LCD colour bit 18 / VOU clock output

LCD_D17 / DVI_HSYNC	O/O	3.3	2	LCD colour bit 17 / VOU line sync output
LCD_D16 / DVI_VSYNC	O/O	3.3	2	LCD colour bit 16 / VOU frame sync output
LCD_D[15:0] / DV_D[15:0]	O/O	3.3	2	lower LCD / Video output colour data
VOU_DEST	O	3.3	2	Signal for selection of either video codec or LCD line drivers
VOU_RST#	O	3.3	2	Signal for resetting an external video codec
VIO (Video Input Unit)				
PTW4	I/O	3.3	2	Portpin PTW4
VIO_D[7:0]	I	3.3	-	Video image input data
VIO_CLK2	I	3.3	-	Video clock input
VIO_HD2	I	3.3	-	Video hsync input
VIO_VD2	I	3.3	-	Video vsync input
VIO_SRC	O	3.3	2	Selection of either camera or video codec input
VIO_RST	O	3.3	2	Reset signal for video device
SPI				
SPI1_SS#	O	3.3	2	Slave select output
SPI1_SCK	O	3.3	2	Clock output
SPI1_MISO	I	3.3	-	Input data from slave
SPI1_MOSI	O	3.3	2	Output data to slave
SPI2_SS#	O	3.3	2	Slave select output
SPI2_SCK	O	3.3	2	Clock output
SPI2_MISO	I	3.3	-	Input data from slave
SPI2_MOSI	O	3.3	2	Output data to slave
SD Card Interface				
SDC_D[3:0]	I/O	3.3	2	SDC data
SDC_CMD	I/O	3.3	2	CMD signal
SDC_CLK	O	3.3	2	SDC Clock output

SDC_CD#	IPU10K	3.3	-	Card detect input
SDC_WP#	IPU10K	3.3	-	Write protect input
I2C				
SCL	I/O PU2K2	3.3	-	I²C clock signal
SDA	I/O PU2K2	3.3	-	I²C data signal
Audio				
AUDIO_MCK	I	3.3	-	Master clock input
AUDIO_BCK	I/O	3.3	2	Sound bit clock
AUDIO_LRC	I	3.3	-	Sound L/R signal
AUDIO_DATI	I	3.3	-	Sound serial input data
AUDIO_DATO	O	3.3	2	Sound serial output data
SPDI	I	3.3	-	PCM input data
SPDO	O	3.3	2	PCM output data
Key Scan Interface				
KEY[10 .. 5]	O	3.3	2	Key scan outputs KEYOUT[5:0]
KEY[4 .. 1]	I	3.3	-	Key scan inputs KEYIN[3:0]
Bus Interface				
A[23 .. 0]	O	3.3	2	Processor address bus
D[15 .. 0]	I/O	3.3	2	Processor data bus
CKIO	O	3.3	2	66 MHz bus clock
WAIT#	IPU 1K	3.3	-	Wait Input
BS#	O	3.3	2	start of a bus cycle
CS4#	O	3.3	2	Chip select output
RD#	O	3.3	2	Read signal
WE0#	O	3.3	2	Write access on even address
WE1#	O	3.3	2	Write access on odd address
RD/WR#	O	3.3	2	Data direction signal
IRQ7	IPU 10K	3.3	-	Interrupt 7 input

IRQ0	IPU 10K	3.3	-	Interrupt 0 input
NMI	I	3.3	-	NMI interrupt
RESI#	IPU 10K	3.3	-	Reset input from carrier board
RESO#	O	3.3	1	Reset output to carrier board
ICIORD#	O	3.3	2	PCMCIA read signal
ICIOWR#	O	3.3	2	PCMCIA write signal
CE1B#	O	3.3	2	PCMCIA chip select for even addresses
CE2B#	O	3.3	2	PCMCIA chip select for odd addresses
IOIS16#	I	3.3	-	PCMCIA 16 bit signal
BAT	-	1.8 - 3.0	< 1 µA	Battery backup input for RTC
+3.3 V	-	-	-	+ 3.3 Volt supply
GND	-	-	-	Ground

7. Technical Characteristics

7.1. Electrical Specifications

Supply voltage	3.3 V, +/-5%
Current consumption	0.35 A max.

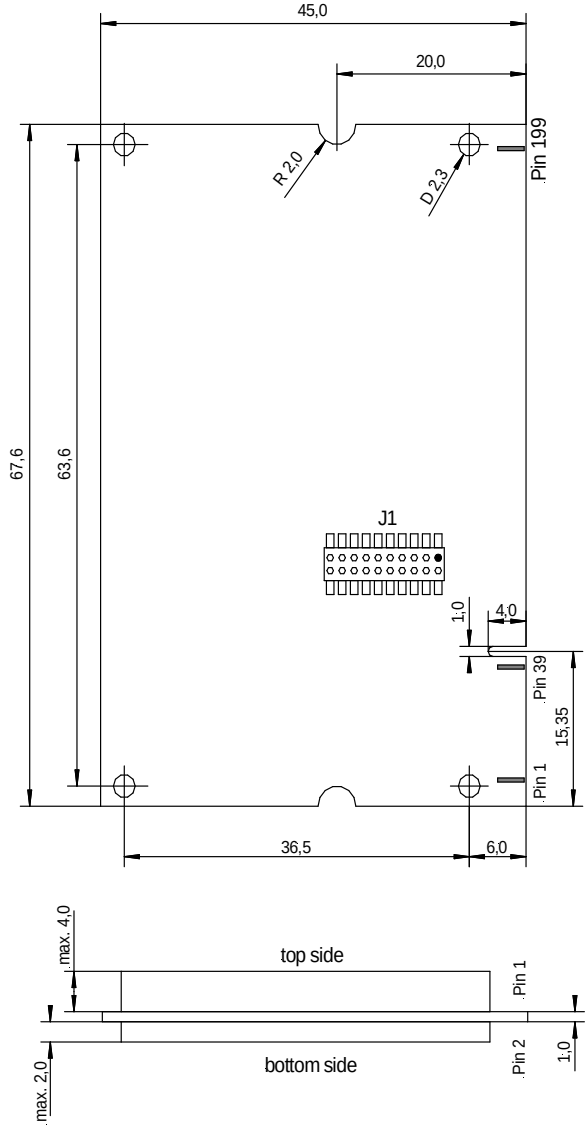
7.2. Environmental Specifications

Operating temperature **Storage temperature**	0 ... +70°C, -40 ... +125°C
Relative humidity	0 ... 95 %, non-condensing

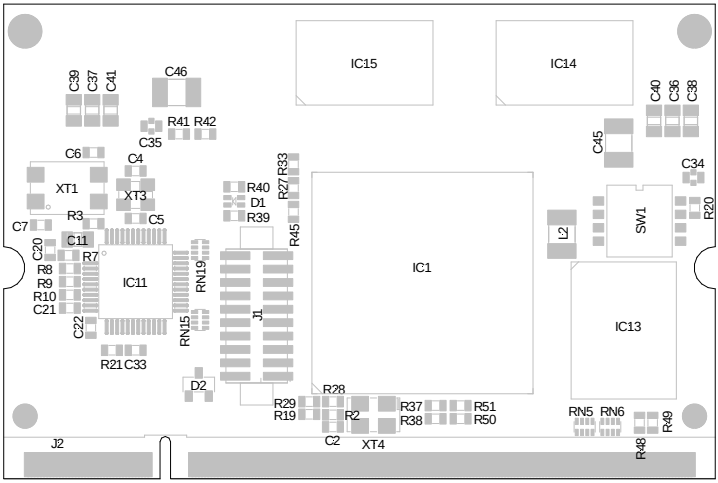
7.3. Mechanical Specifications

Weight	approx. 16 g
Board	Glasepoxi FR-4, UL-listed, 8 layers
Dimensions	67.6 mm x 45.0 mm x 7.0 mm

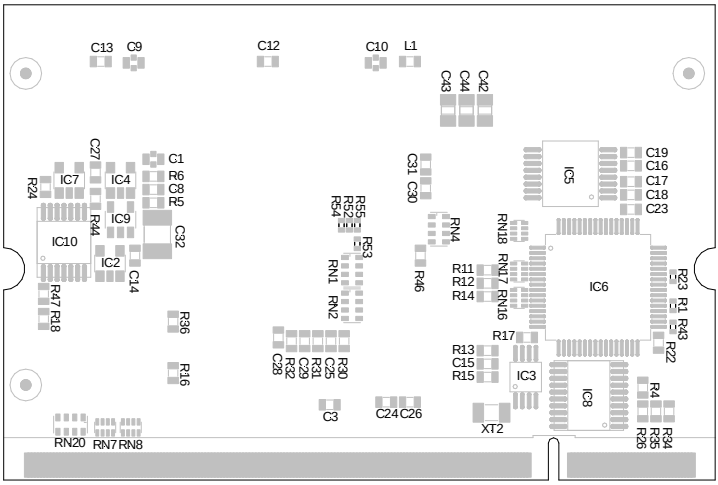
7.3.1. Dimensional Drawing



7.3.2. Top View



7.3.3. Bottom View



8. References

[1] SH7722
Hardware Manual
Renesas 32-Bit RISC Microcomputer SH7780 Series R8A7722
Revision 1.00, June 20, 2007
Renesas Technology

[2] DM9000B
Ethernet Controller With General Processor Interface
Datasheet
Final Version: DM9000B-13-DS-F01, February 1, 2008
Davicom

[3] ISP1160
Embedded Universal Serial Bus Host Controller
Rev. 05, 24 December 2004
Philips

[4] TSC2007
1.2V to 3.6V, 12-Bit, Nanopower, 4-Wire Micro Touch Screen Controller with I2C™ Interface
SBAS405-March 2007
Texas Instruments